

PAGE	TITLE
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[illegible]

GIGABYTE™			
Title COVER SHEET			
Size	Document Number		Rev
Custom	GA-A75M-S2V		1.0
Date:	Friday, June 10, 2011	Sheet	1 of 29

Component value change history

Version: 1.0

P-Code: U98126-0

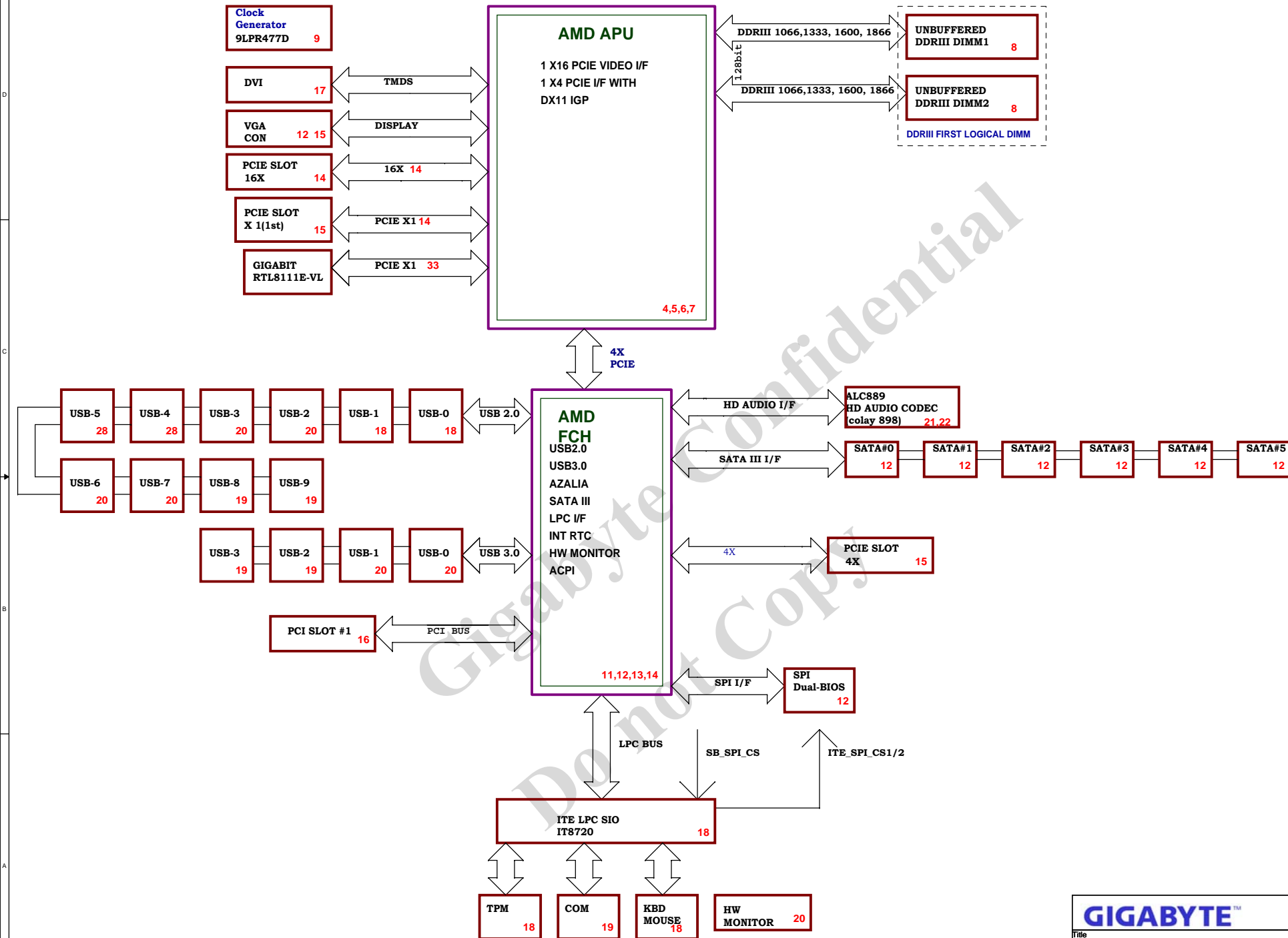
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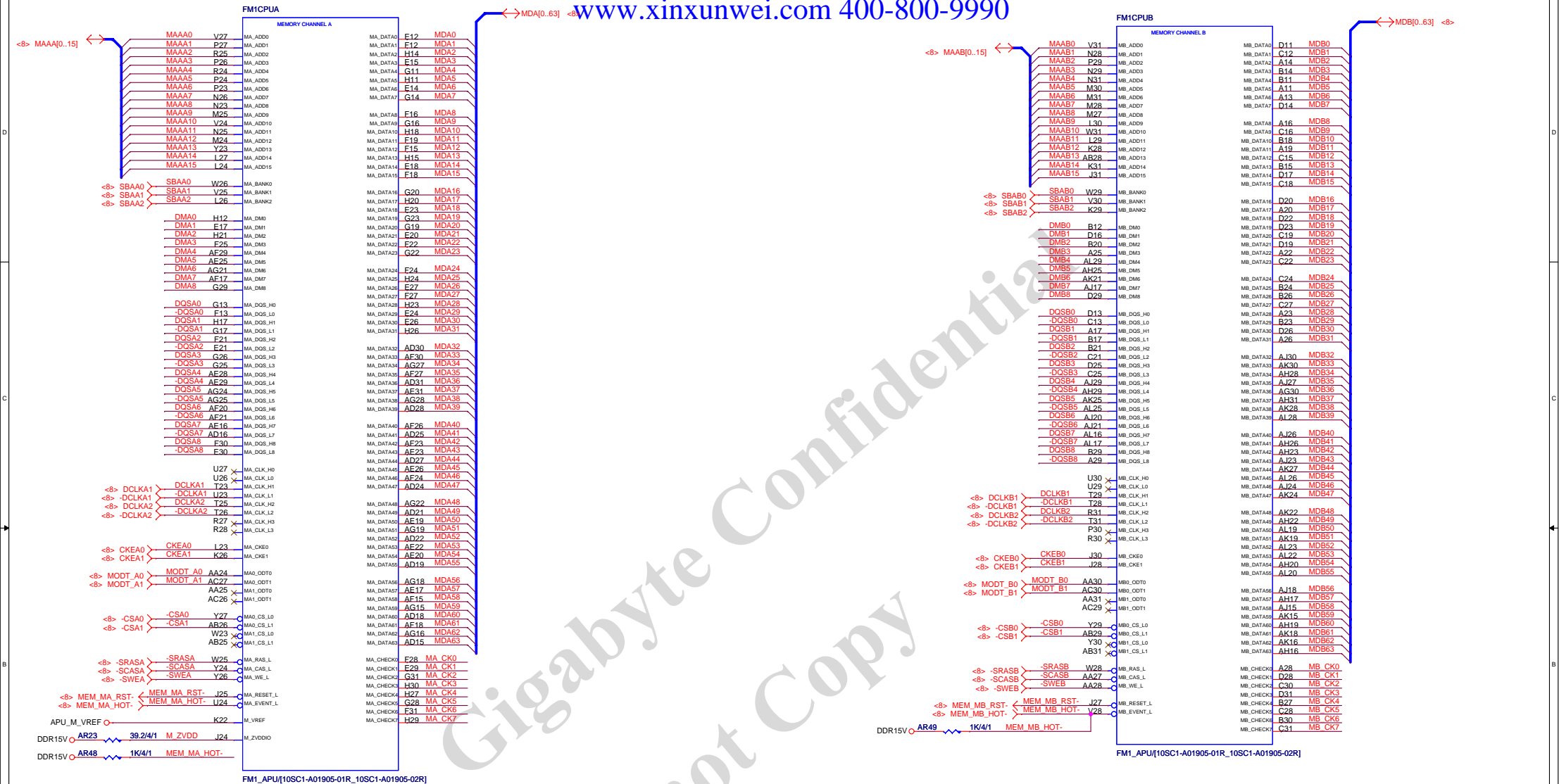
Circuit or PCB layout change for next version

[illegible]

AMD Fusion D3 DESKTOP REFERENCE DESIGN

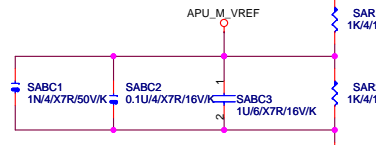
www.xinxiunwei.com 400-800-9990



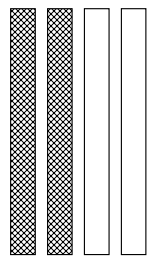


CPUVREF

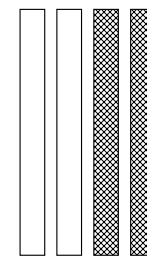
40 MILS WIDTH



MEM CHA



MEM CHB

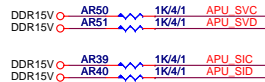


GIGABYTE™

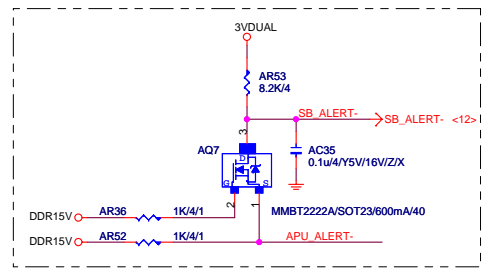
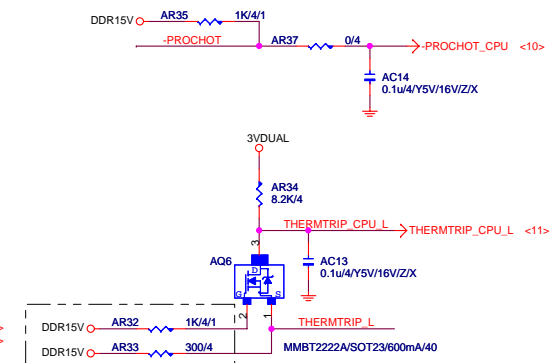
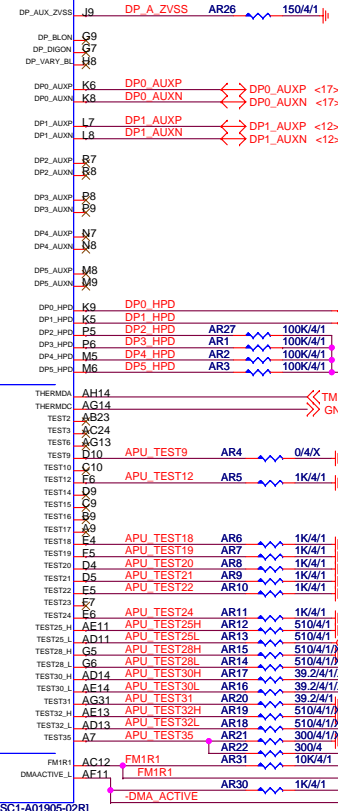
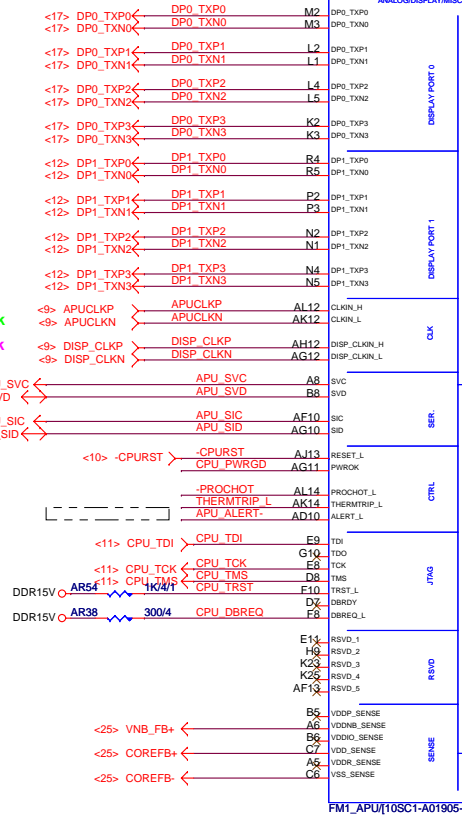
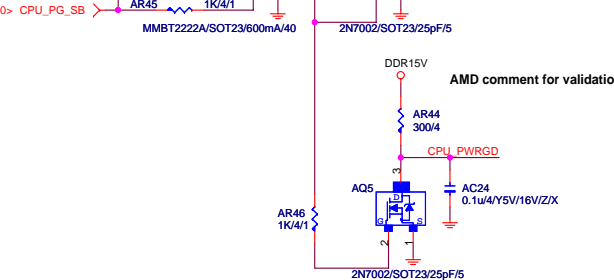
CPU DDRIII MEMORY

Size Custom Document Number GA-A75M-S2V Rev 1.0

Date: Friday, June 10, 2011 Sheet 4 of 29

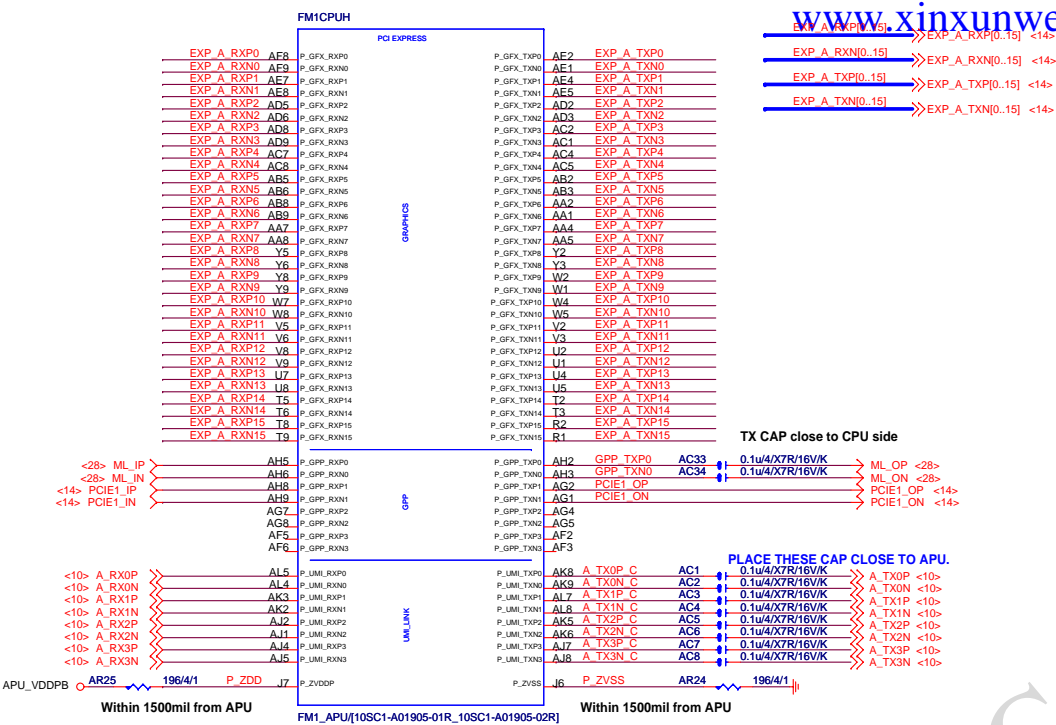


DP Non-Spread 100Mhz clock



TEST35: high=>HDMI enable,
low=>HDMI disable.





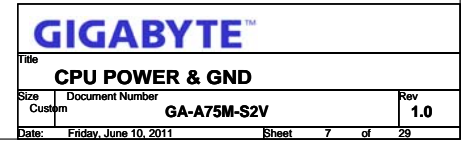
TX CAP close to CPU side

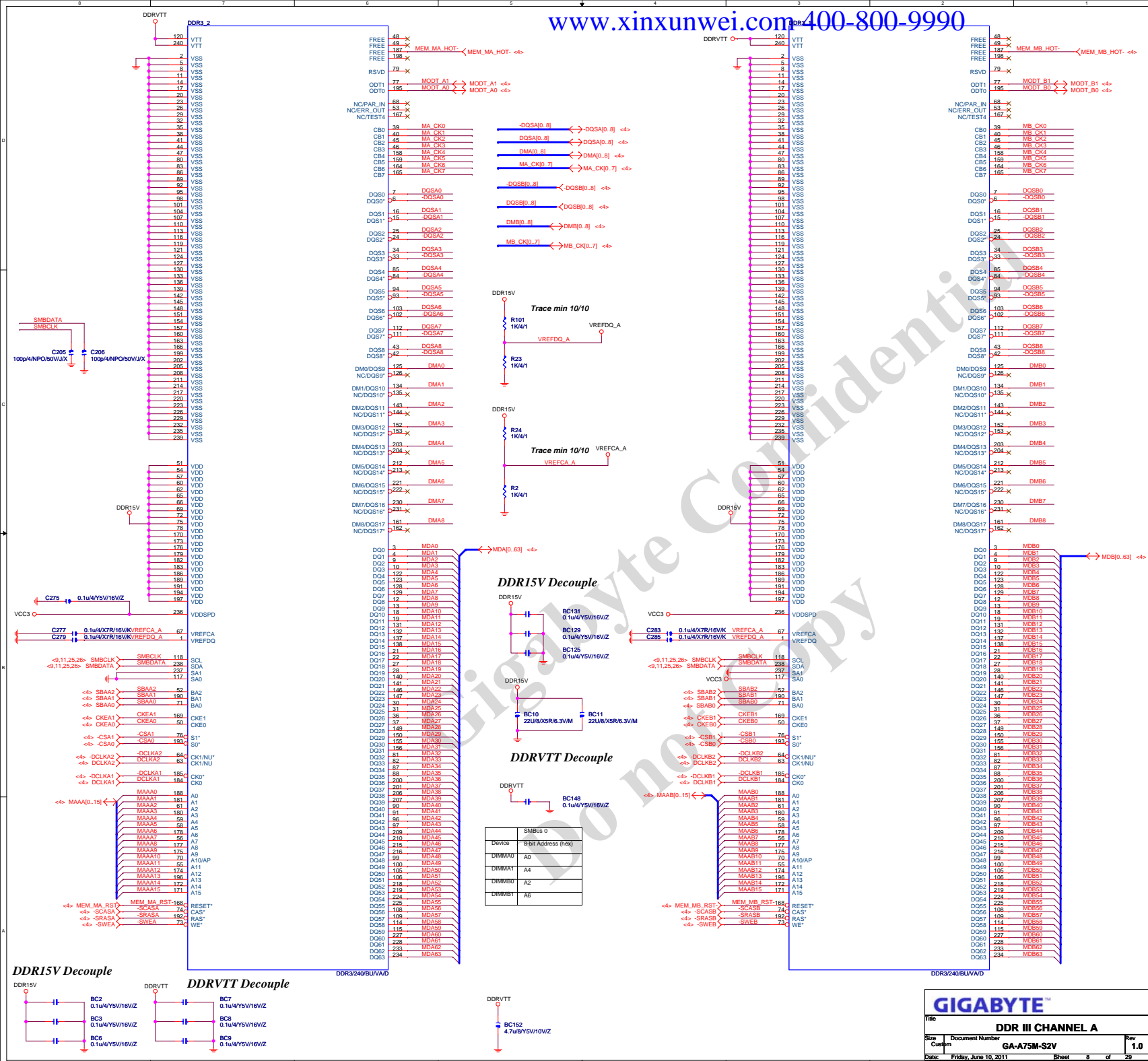
AH2 GPP_TXP0 AC33 0.1u/4X7R/16V/K
AH3 GPP_TXN0 AC34 0.1u/4X7R/16V/K
AG2 PCIE1_OP
AG1 PCIE1_ON
AG4
AG5
AF2
AF3

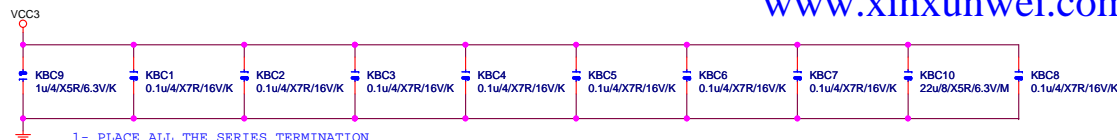
ML_OP <28>
ML_ON <28>
PCIE1_OP <14>
PCIE1_ON <14>

PLACE THESE CAP CLOSE TO APU.

AK8 A_TX0P C AC1 0.1u/4X7R/16V/K A_TX0P <10>
AK9 A_TX0N C AC2 0.1u/4X7R/16V/K A_TX0N <10>
AL7 A_TX1P C AC3 0.1u/4X7R/16V/K A_TX1P <10>
AL8 A_TX1N C AC4 0.1u/4X7R/16V/K A_TX1N <10>
AK5 A_TX2P C AC5 0.1u/4X7R/16V/K A_TX2P <10>
AK6 A_TX2N C AC6 0.1u/4X7R/16V/K A_TX2N <10>
AJ7 A_TX3P C AC7 0.1u/4X7R/16V/K A_TX3P <10>
AJ8 A_TX3N C AC8 0.1u/4X7R/16V/K A_TX3N <10>







1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE



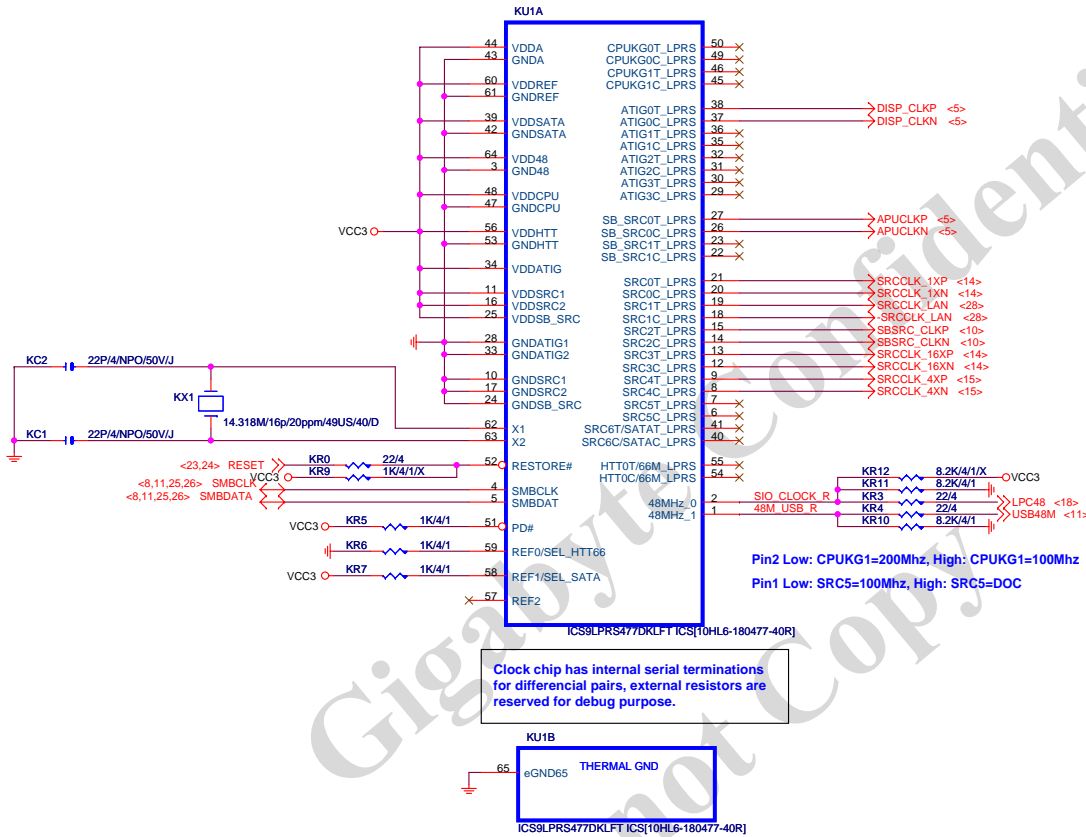
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

NO.0000 INPUT TABLE

NO.0000	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* the GFX_REFCLK input is required for all cases



watch dog --
RESTORE# 接 RESET

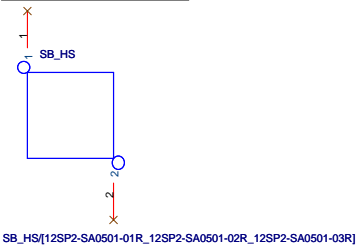
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

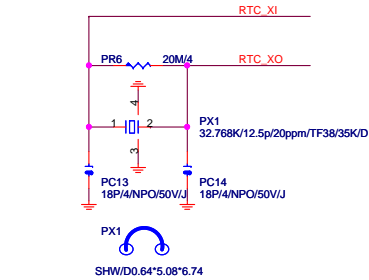


PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK

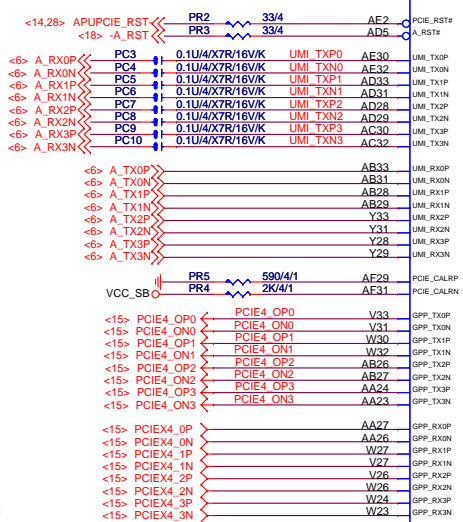


SB_HS[12SP2-SA0501-01R_12SP2-SA0501-02R_12SP2-SA0501-03R]



SHW/D0.64*5.08*6.74

For APU PCI E devices.



VCC_SB PR4 590/4/1 2K/4/1

SBSRC_CLKP PR5 2K/4/1

SBSRC_CLKN PR5 2K/4/1

DISP_CLKP PR5 2K/4/1

DISP_CLKN PR5 2K/4/1

APU_CLKP PR5 2K/4/1

APU_CLKN PR5 2K/4/1

SUT_GFX_CLKP PR5 2K/4/1

SUT_GFX_CLKN PR5 2K/4/1

GPP_CLKP PR5 2K/4/1

GPP_CLKN PR5 2K/4/1

GPP_CLKP PR5 2K/4/1

GPP_CLKN PR5 2K/4/1

GPP_CLKP PR5 2K/4/1

GPP_CLKN PR5 2K/4/1

GPP_CLKP PR5 2K/4/1

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GPP_CLKN PR5 2K/4/1

GPP_CLKP PR5 2K/4/1

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GPP_CLKP PR5 2K/4/1

GPP_CLKN PR5 2K/4/1

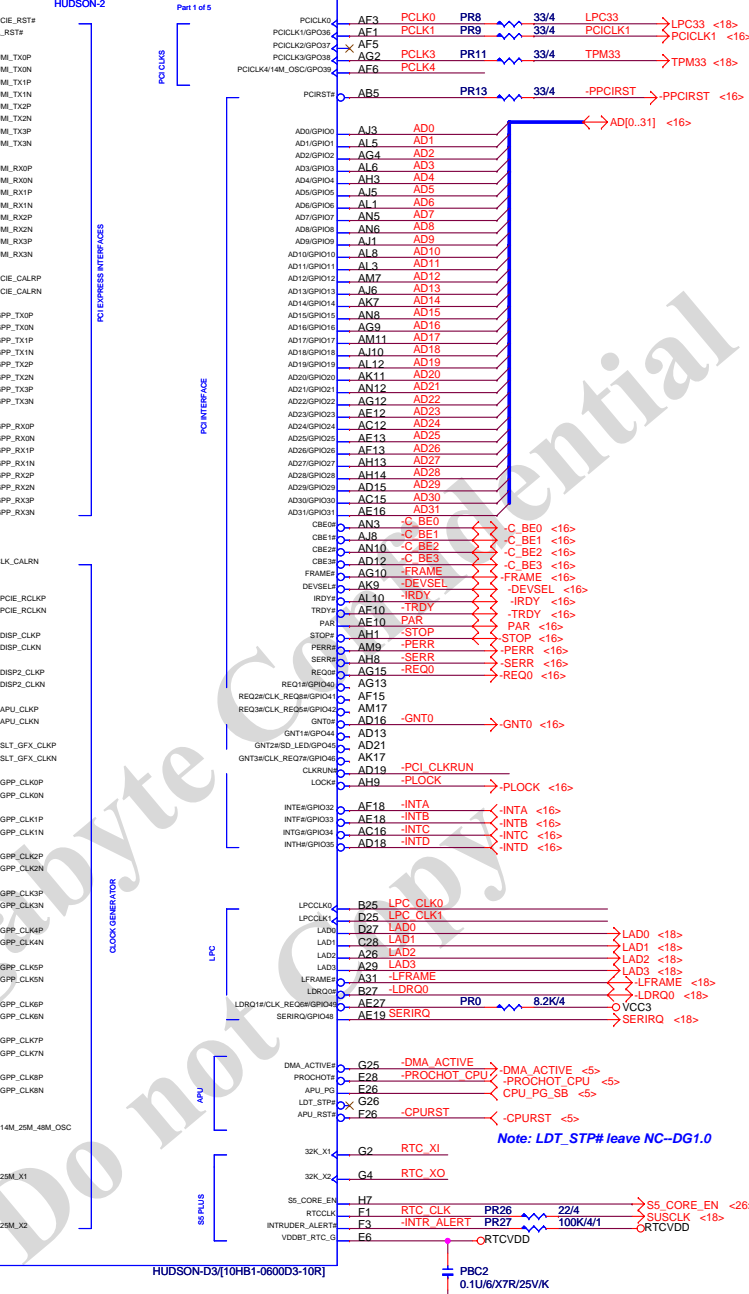
GPP_CLKP PR5 2K/4/1

GPP_CLKN PR5 2K/4/1

GPP_CLKP PR5 2K/4/1

GPP_CLKN PR5 2K/4/1

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Note: LDT_STP# leave NC--DG1.0

SS_CORE_EN PR26 22/4

RTC_CLK PR27 100K/4/1

INTR_ALERT PR27 100K/4/1

VDDBT_RTC PR27 100K/4/1

RTC_CLK PR27 100K/4/1

INTR_ALERT PR27 100K/4/1

VDDBT_RTC PR27 100K/4/1

RTC_CLK PR27 100K/4/1

INTR_ALERT PR27 100K/4/1

VDDBT_RTC PR27 100K/4/1

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

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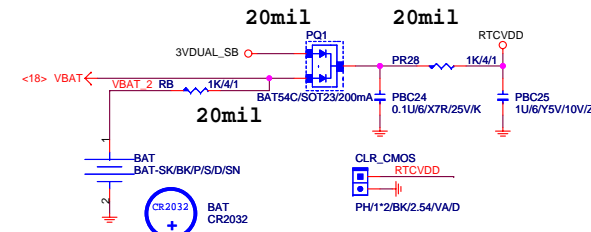
Low: Force PCIE GEN1, Up: Allow PCIE GEN2

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

Low: Force PCIE GEN1, Up: Allow PCIE GEN2

Low: Force PCIE GEN1, Up: Allow PCIE GEN2



CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

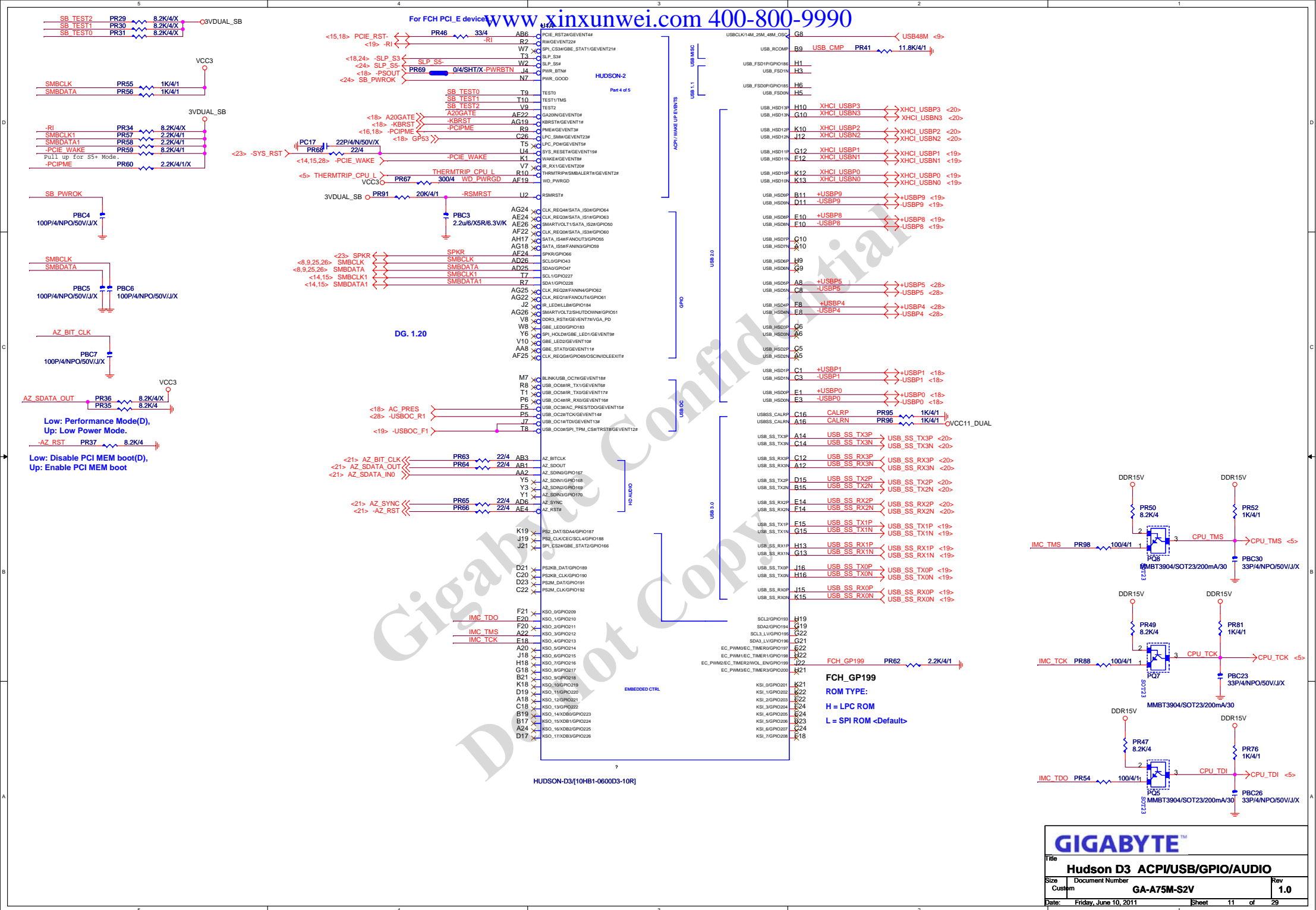
GIGABYTE

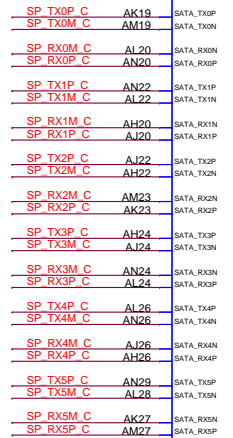
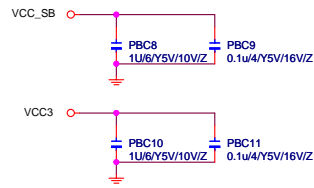
Hudson D3 PCIE/PCI/CPU/LPC

GA-A75M-S2V

Rev 1.0

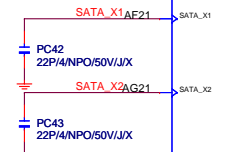
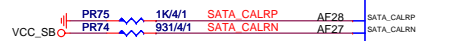
Friday, June 10, 2011





SATA 6-7 for Hudson D4.

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U1



HUDSON-2

Part 2 of 5

SD CARD

GBE LAN

SERIAL ATA

SATA 6-7 for Hudson D4.

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U1

SATA LED

SATA X1

SATA X2

FCH ALERT

HUDSON-D3(10HBI-0600D3-10R)

SATA3_0

SATA3_1

SATA3_2

SATA3_3

SATA3_4

SATA3_5

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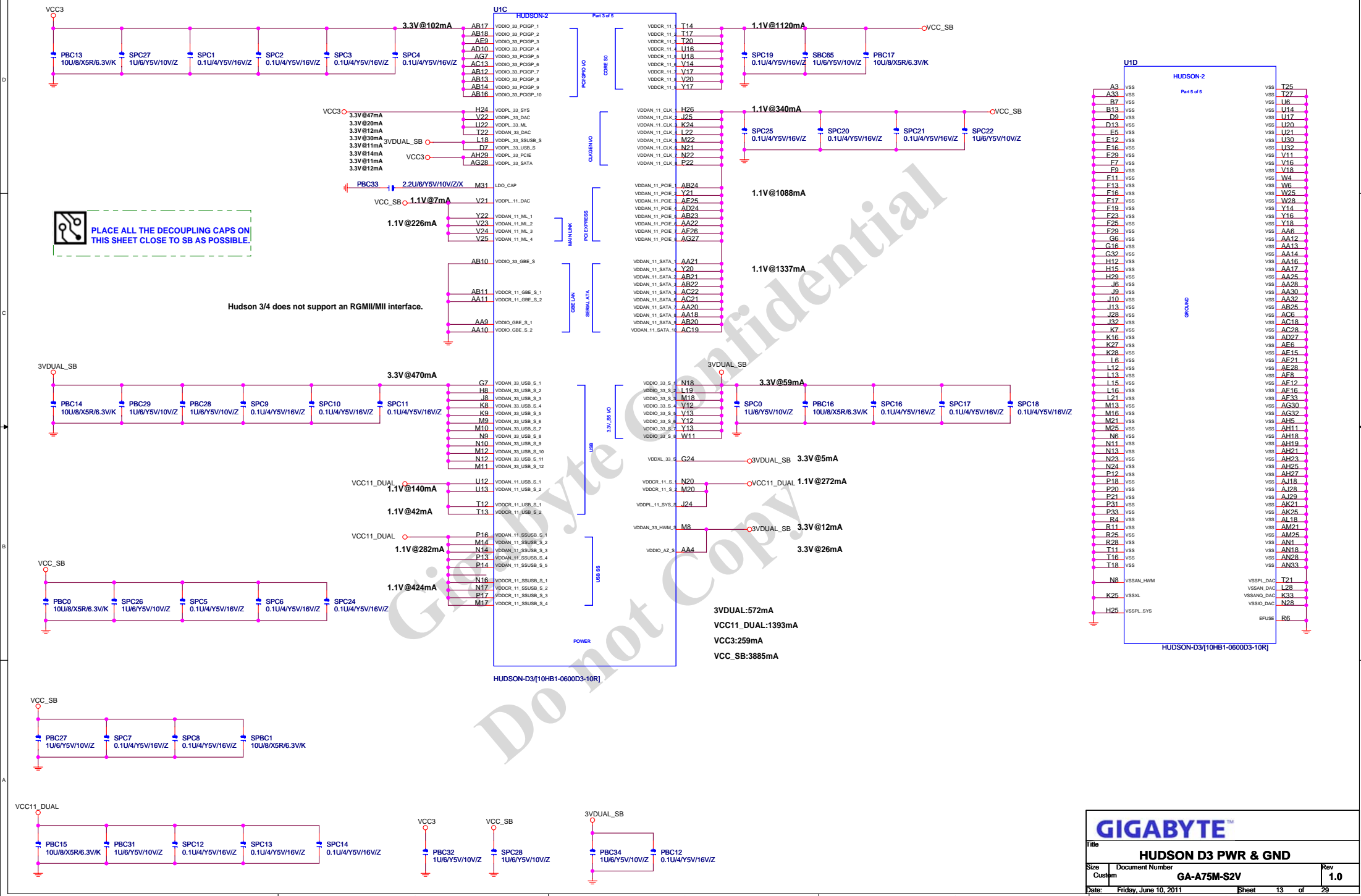
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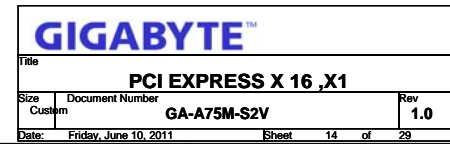
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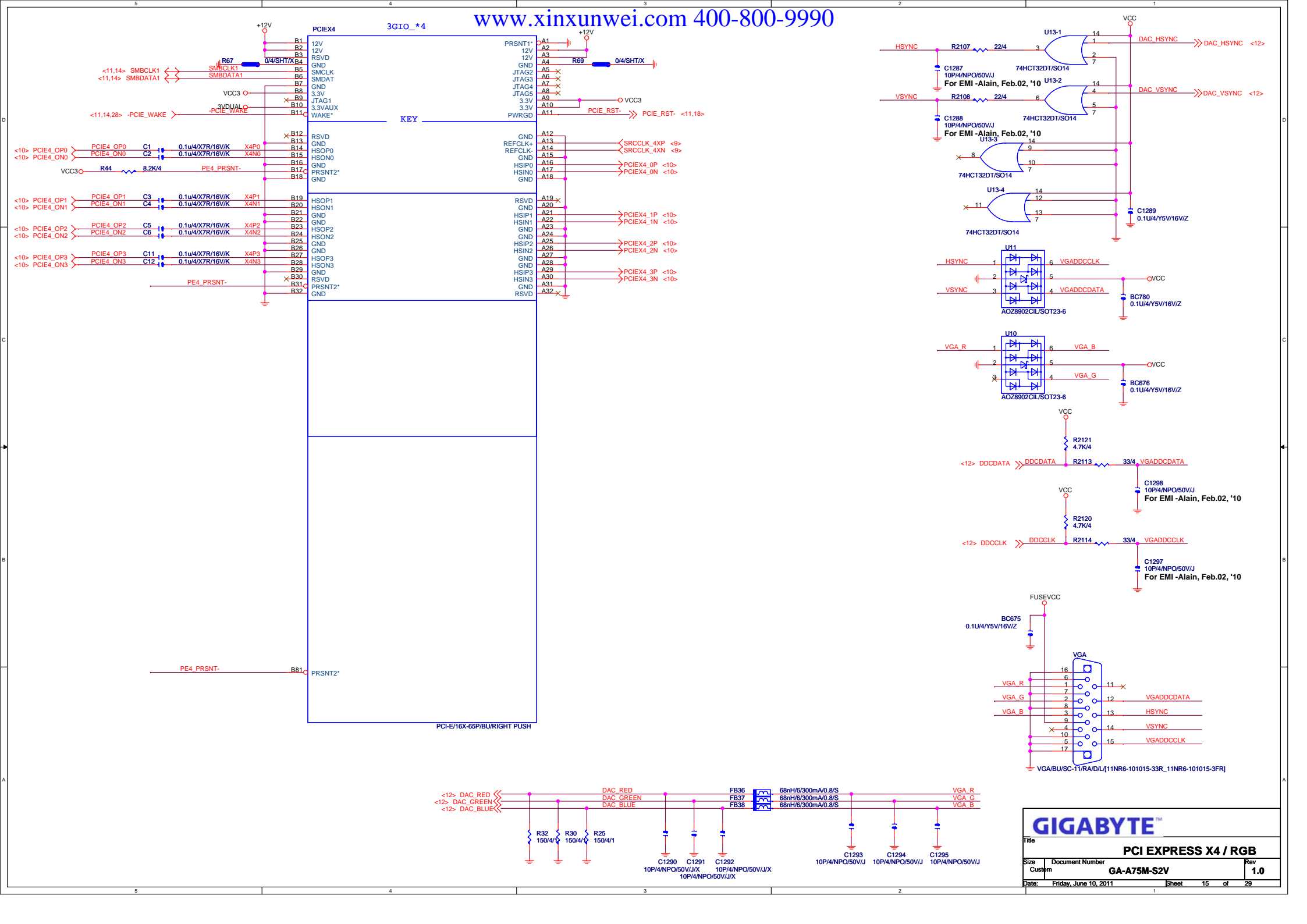
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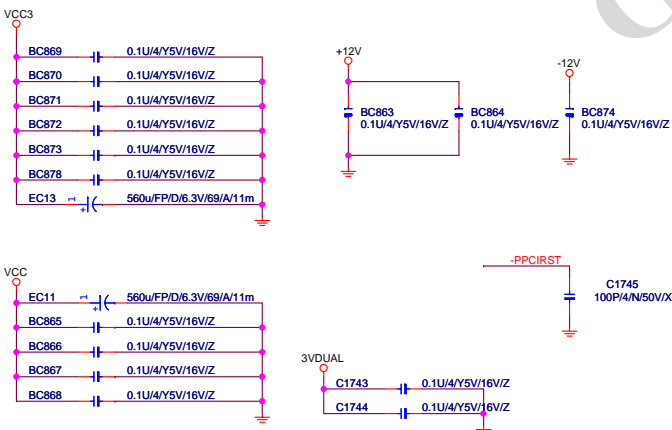
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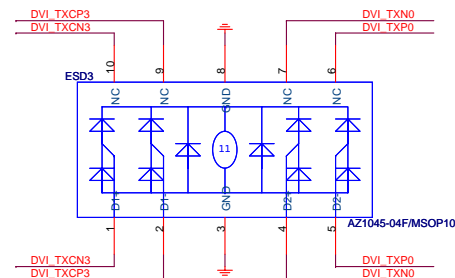
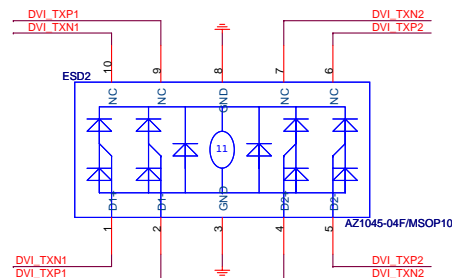
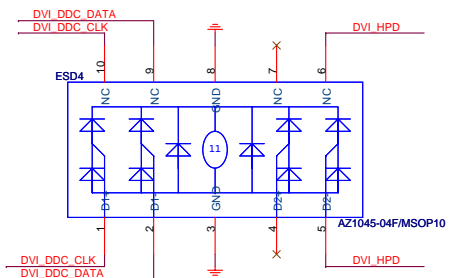
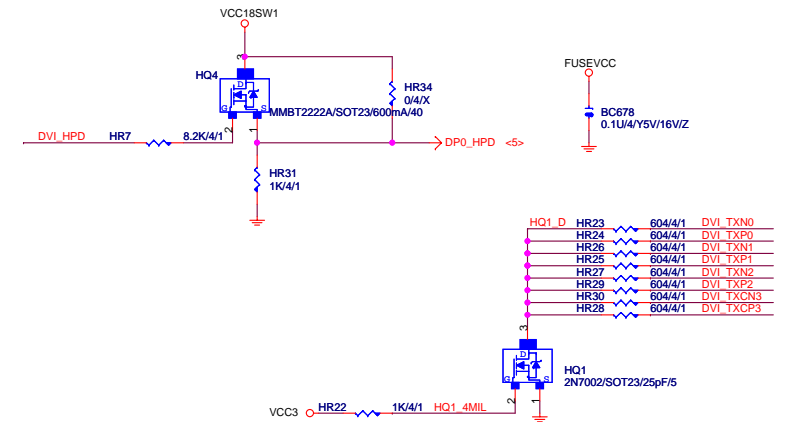
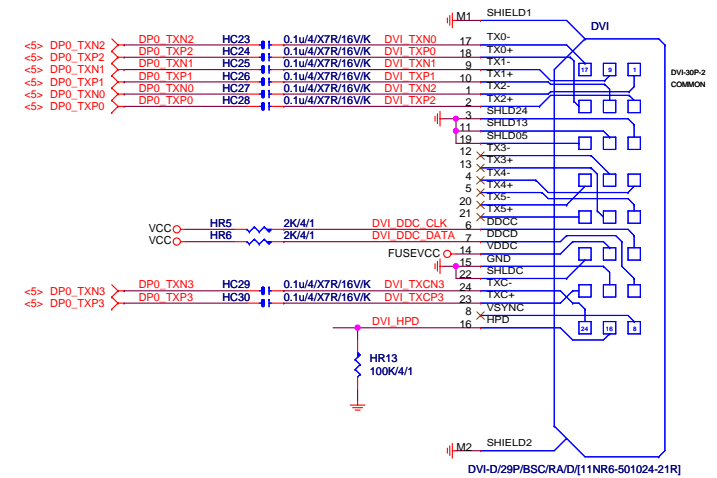
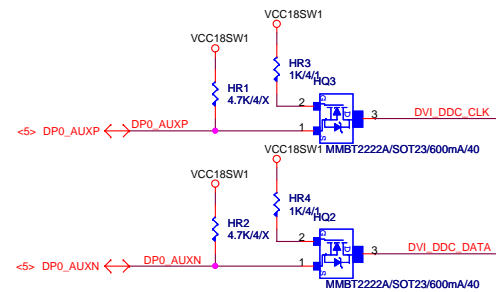
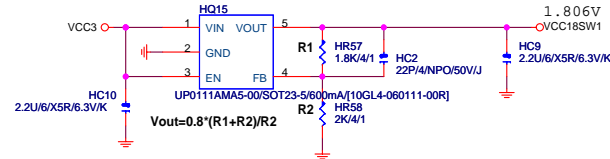
SATA3_294

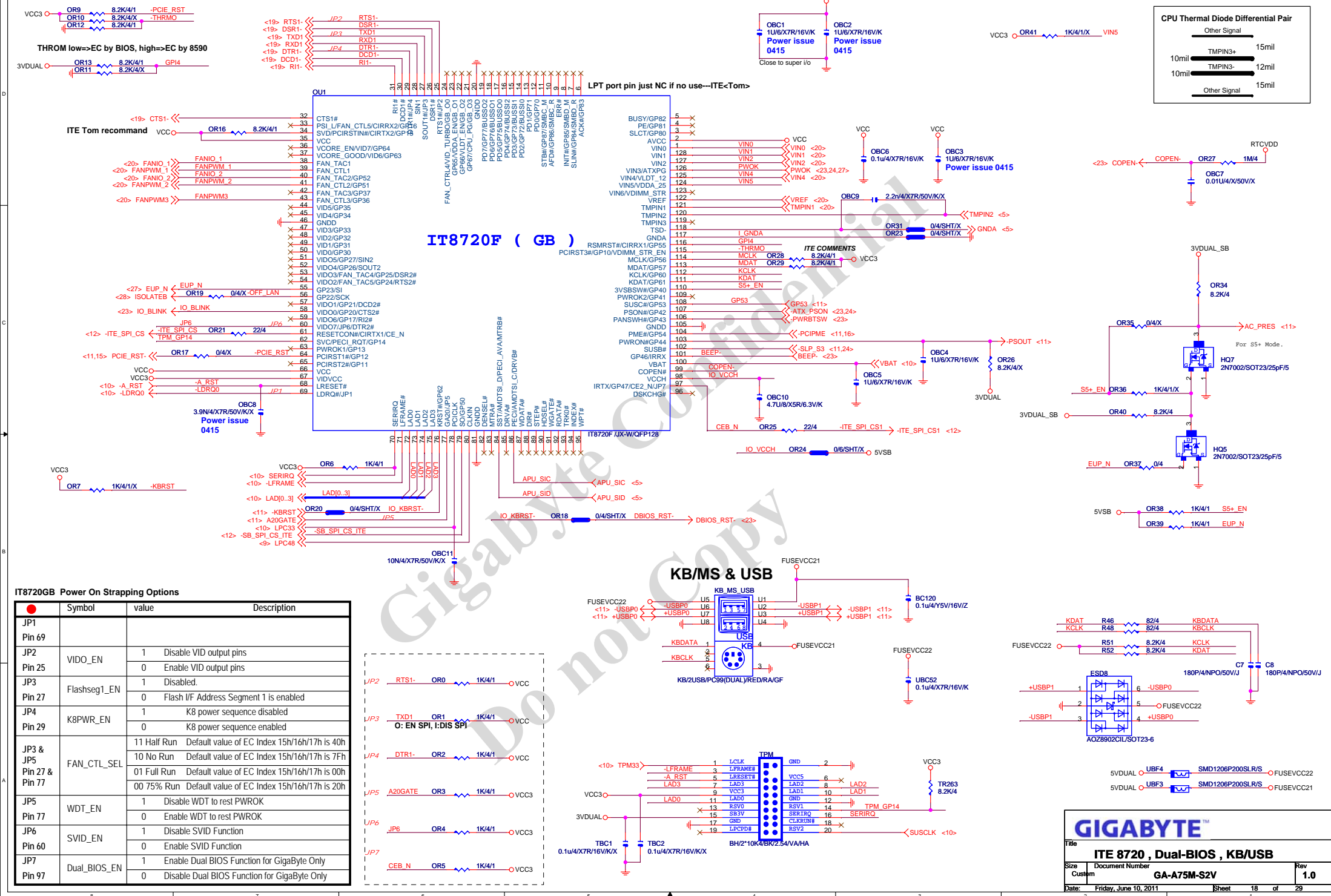


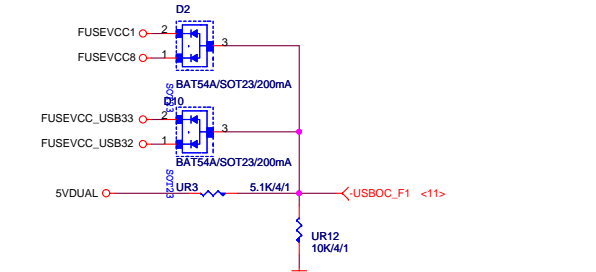
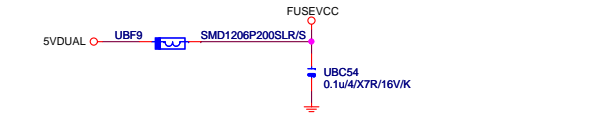
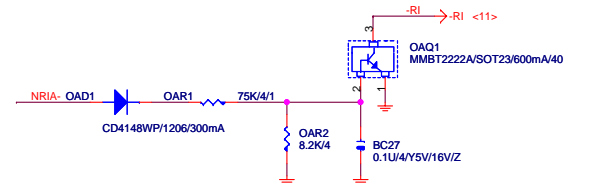
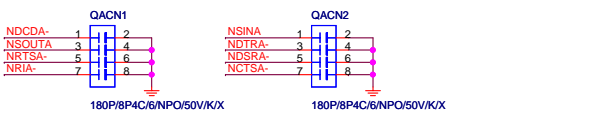
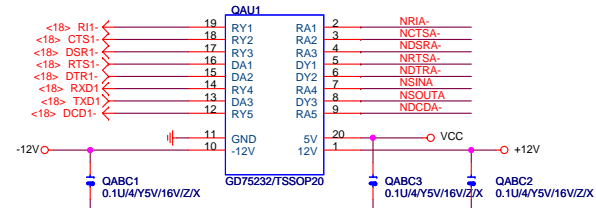




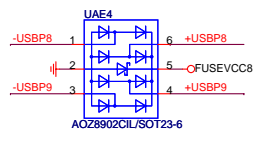
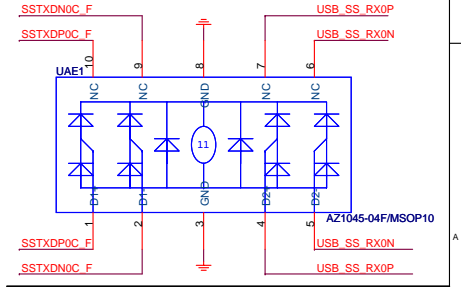
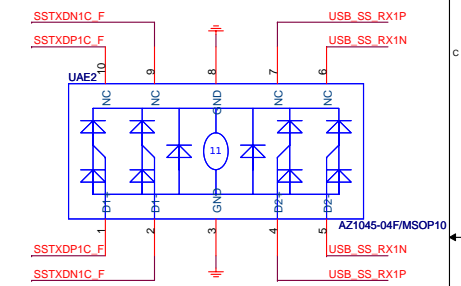
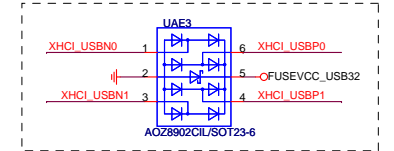
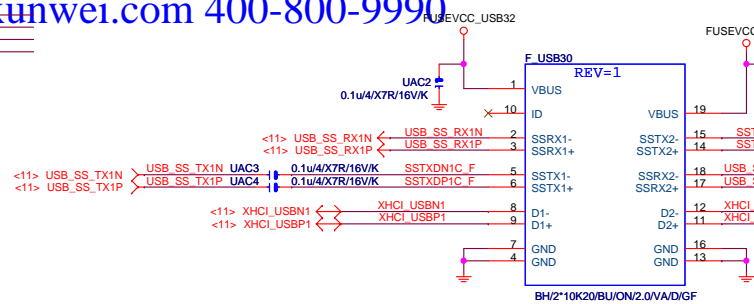
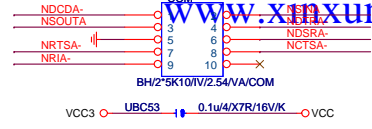
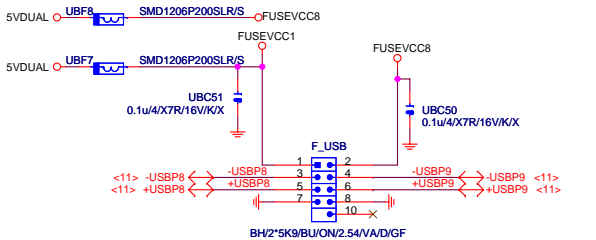








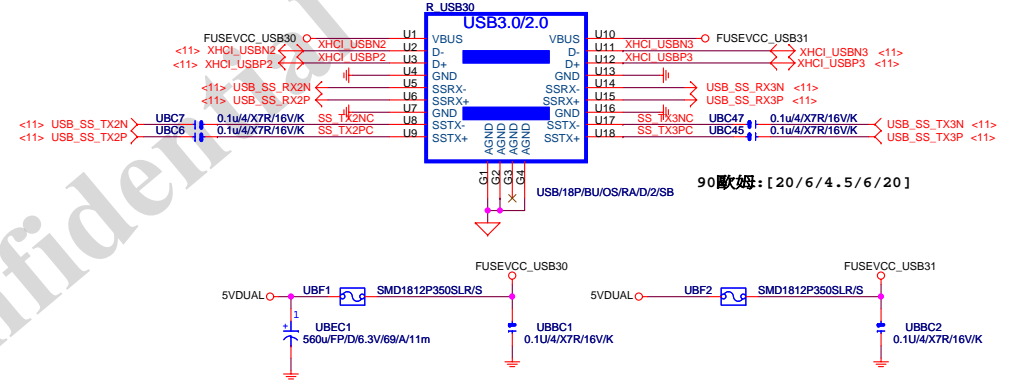
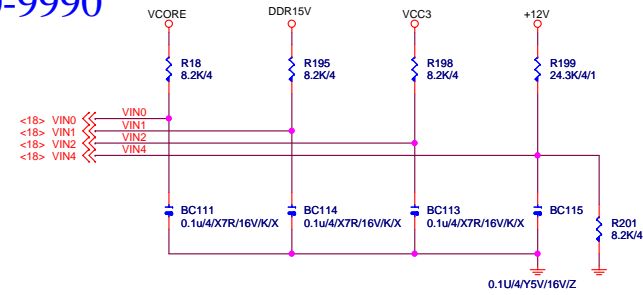
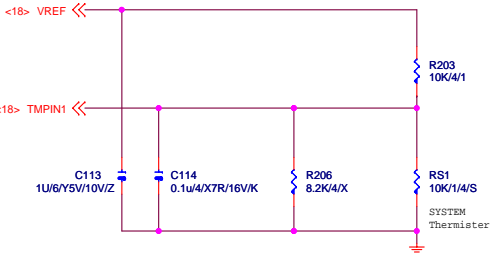
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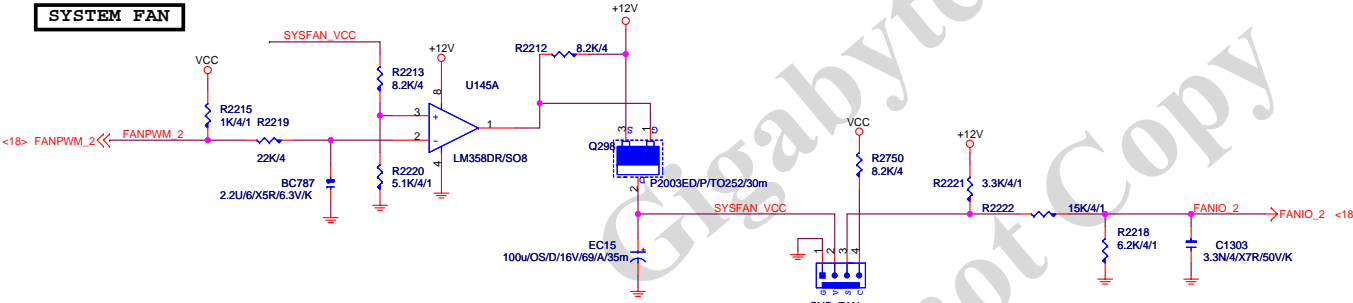
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Hardware Monitor circuits

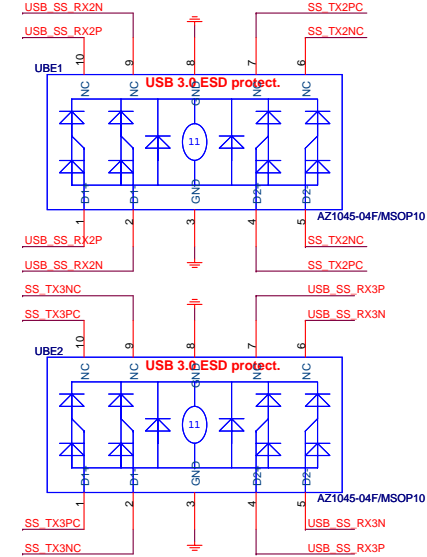
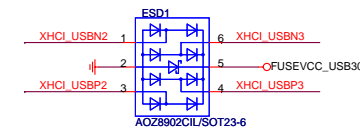
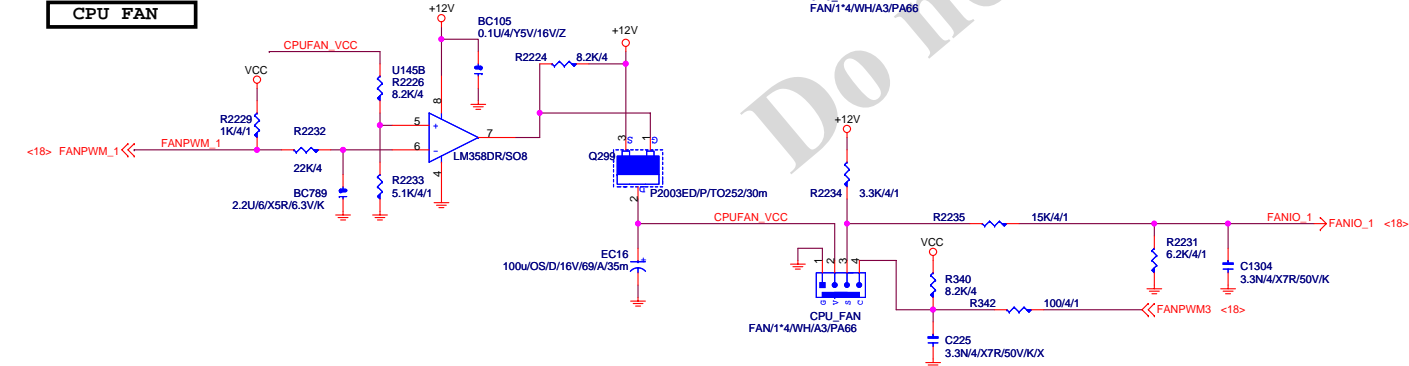
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SYSTEM FAN

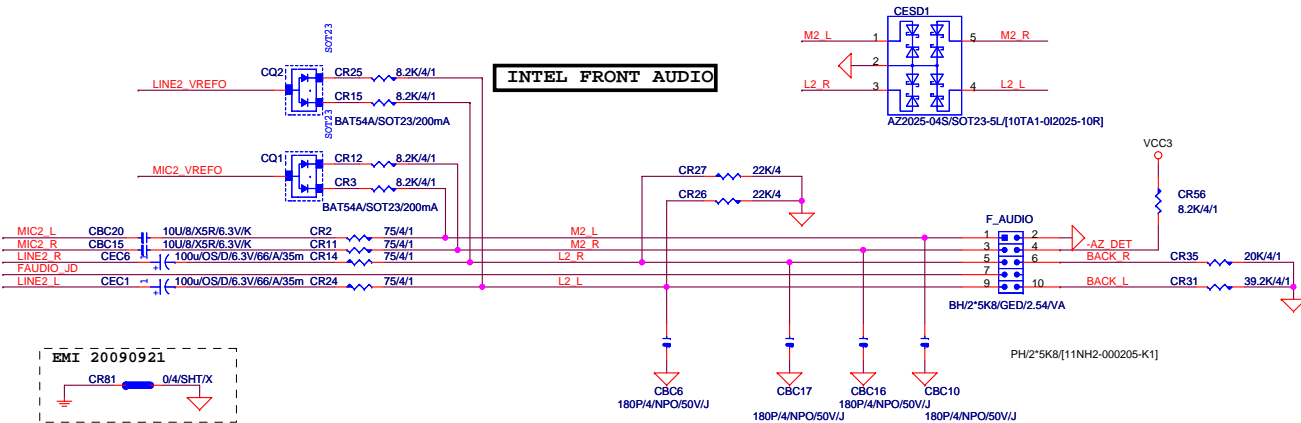
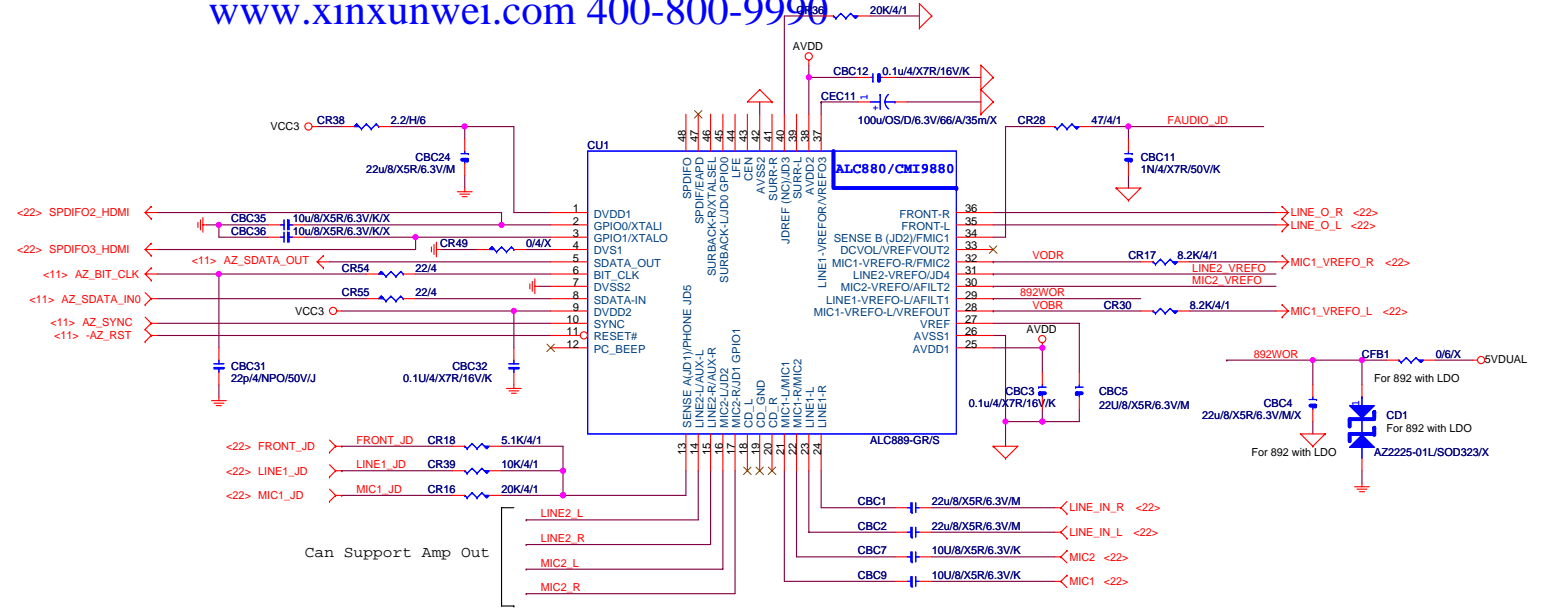


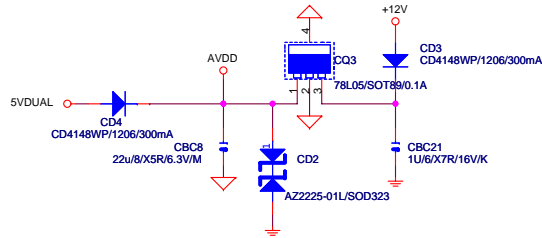
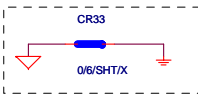
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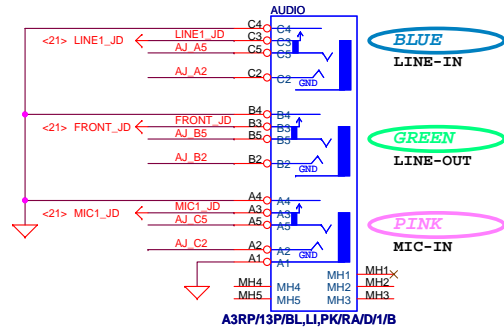
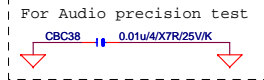
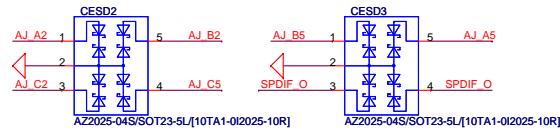
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FAN , HWMO , R_USB30			
Size	Document Number	Rev	
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	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm



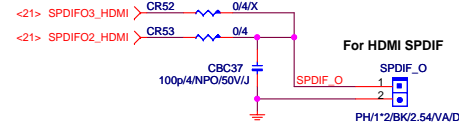


For ESD PROTECT DIODE



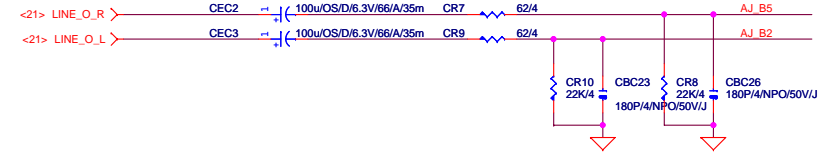
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SPDIF



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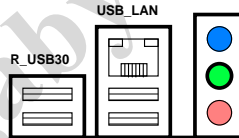
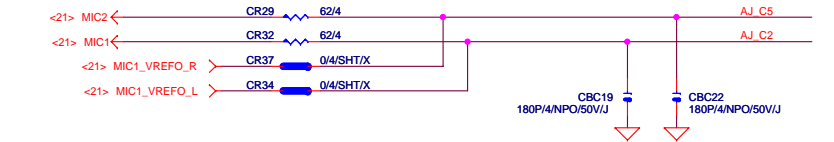
LINE OUT
FRONT OUT



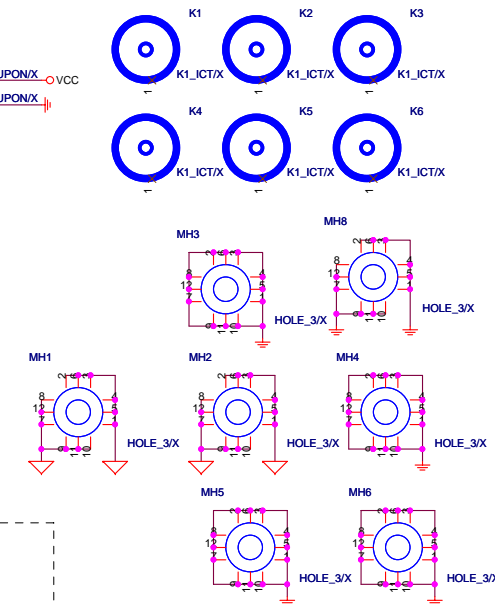
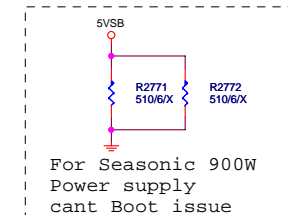
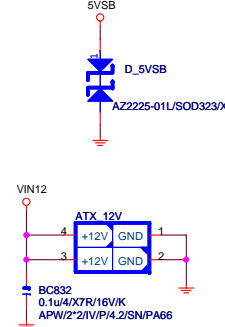
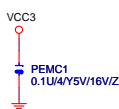
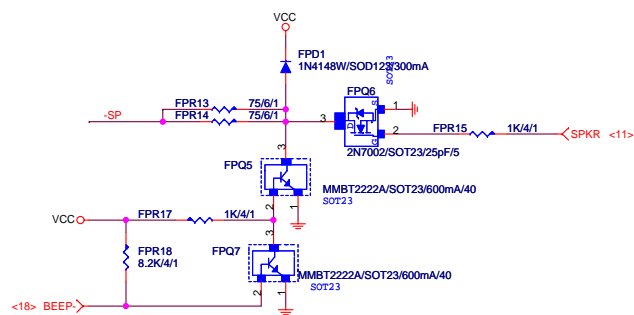
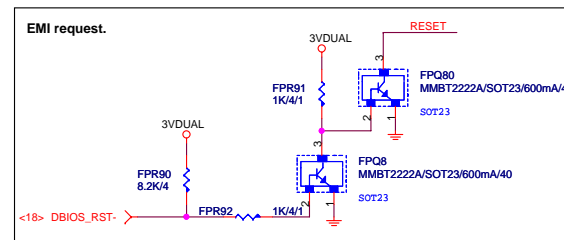
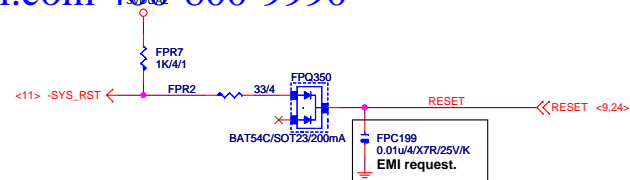
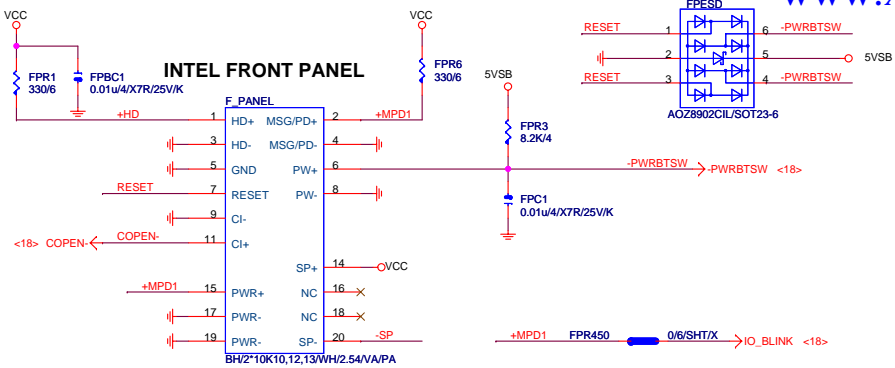
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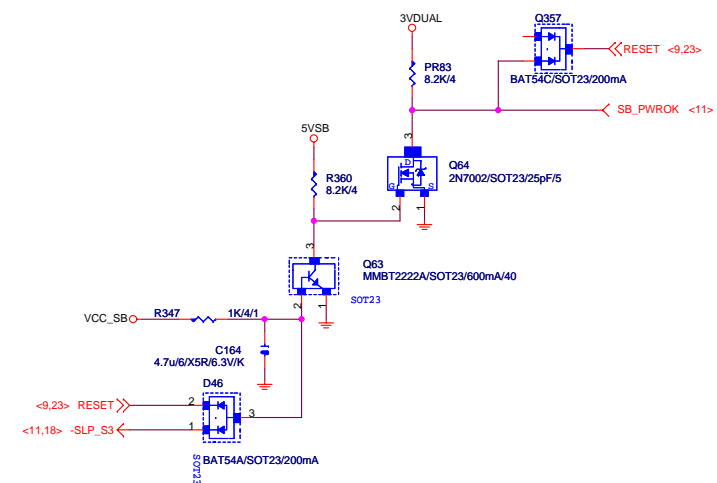
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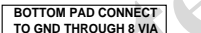


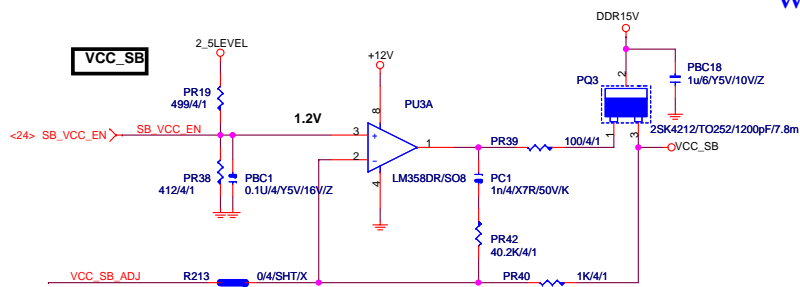
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AUDIO JACK			
Size	Document Number	Rev	
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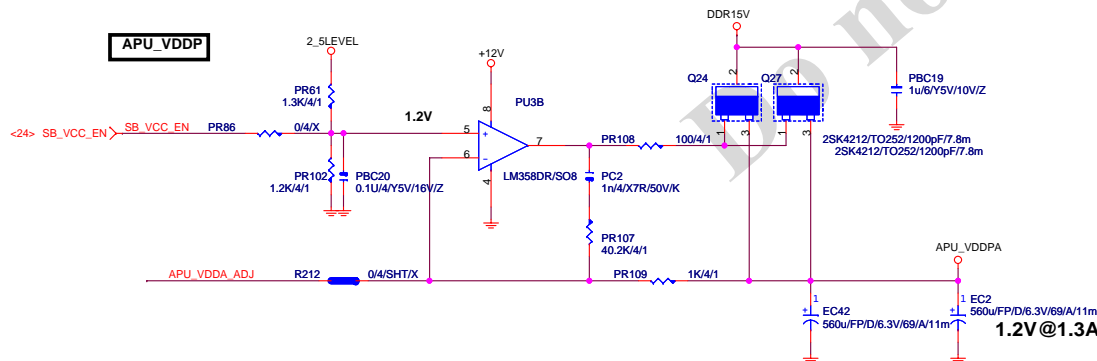
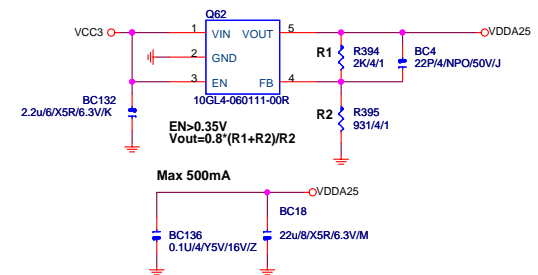
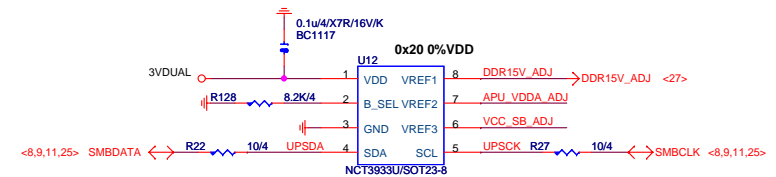
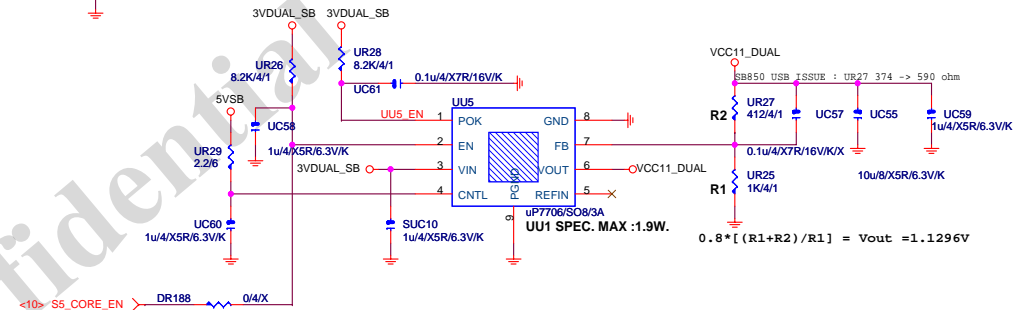
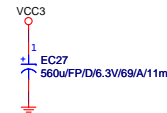
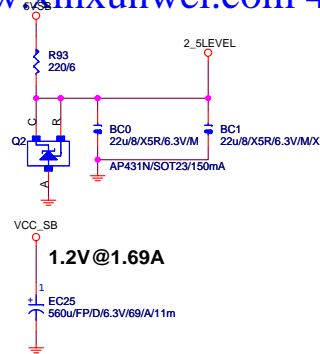
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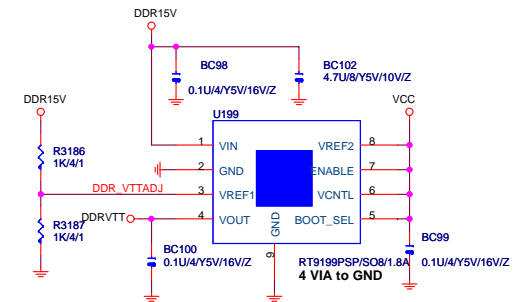
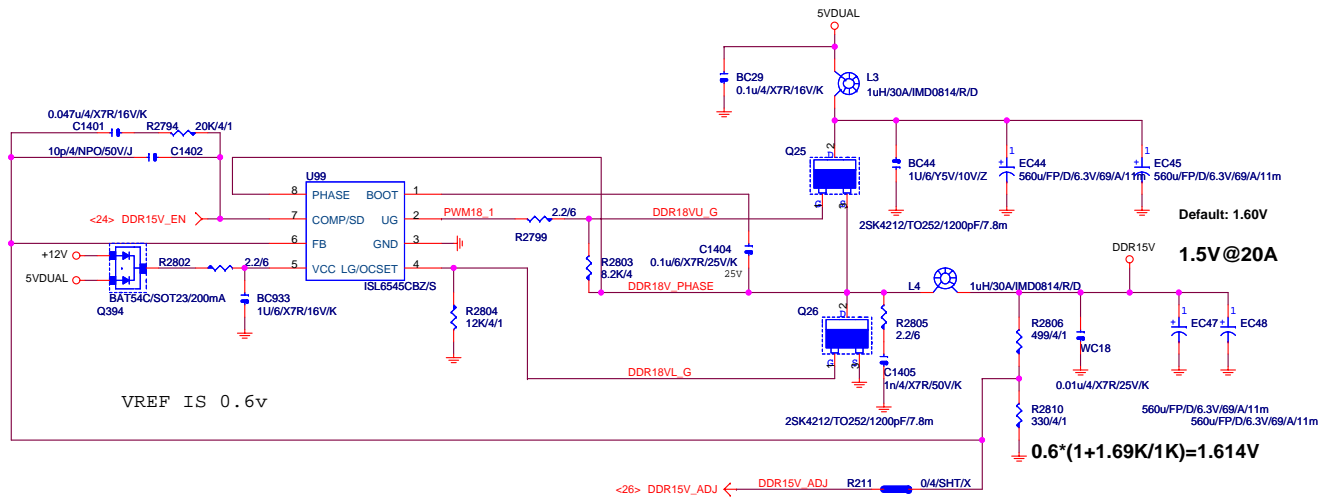
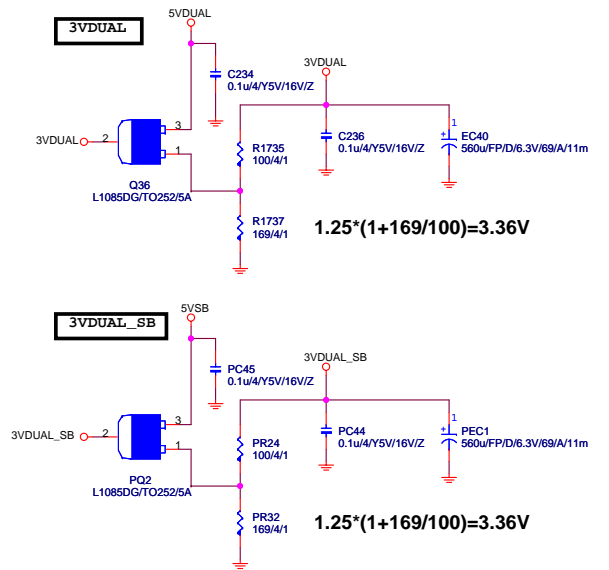
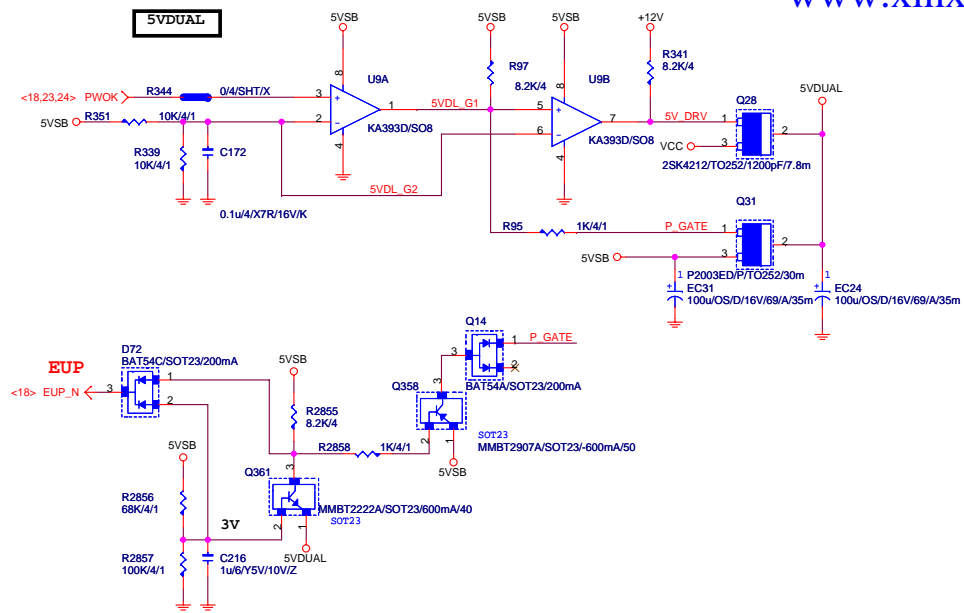




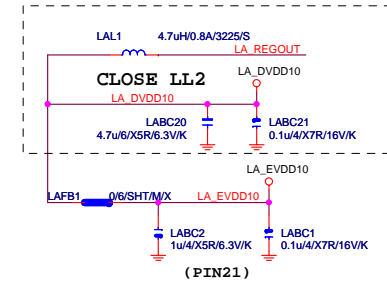


VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V





	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

[illegible]